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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,168	12/06/2003	James R. Lundberg	CNTR.2197	2861

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EXAMINER	
CHO, JAMES HYONCHOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 08/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,168	LUNDBERG, JAMES R.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,9,10,12,13 and 18-20* is/are rejected.

7)☒ Claim(s) *5,6,8,11,14-17,21 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03,3,4,5,6/05,1/06*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

The co-pending application data in paragraph [0002] needs to be update with proper serial number and the patent number as following; U.S. Patent Serial No. 10/730,703 filed 12/09/2003, now U.S. Patent No. 6,965,254.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 7, 9-10, 12-13 and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Partovi H. et al. ("Flow-through latch and edge-triggered flip-flop hybrid elements", SOLID-STATE CIRCUITS CONFERENCE, 1996).

Regarding claim 1, Fig. 8 of Partovi H. et al. teaches a dynamic logic return-to-zero (RTZ) latching mechanism, comprising: a complementary pair of evaluation devices (first PMOS whose gate coupled to CLK and NMOS whose gate coupled to a three series connected inverter) responsive to a clock signal (CLK); a dynamic evaluator (NMOS coupled to D), coupled between the complementary pair of evaluation devices at a pre-charged node (node coupled to the first PMOS), that evaluates a logic function (buffer) based on at least one input data signal (D); delayed inversion logic (three

inverter connected in series provides delay) that receives the clock signal and that outputs an evaluation complete signal being a delayed and inverted version of the clock signal (the output of three series connected inverters) ; and latching logic (full latch comprising two inverters coupled to Q), responsive to the evaluation complete signal and the state of the pre-charged node, that asserts the logic state of an output node based on the state of the pre-charged node during an evaluation period between an operative edge of the clock signal and the next edge of the evaluation complete signal, and that returns the output node to zero between evaluation periods (samples the data on the rising edge of the clock and being reset through PR1 after a predetermined delay period where the output Q is returns to zero when reset by PR1; last paragraph on page 138).

Regarding claim 2, Fig. 8 of Partovi H. et al. teaches the dynamic logic RTZ latching mechanism of claim 1, wherein the complementary pair of evaluation devices comprises: a P-channel device (first PMOS whose gate is coupled to CLK) having a gate receiving the clock signal (CLK) and a drain and source coupled between a source voltage and the pre-charged node (first PMOS coupled between power source and precharge node); and an N-channel device having a gate receiving the clock signal (NMOS whose gate coupled to CLK via a three series connected inverter and coupled between evaluator NMOS and ground) and a drain and source coupled between the dynamic evaluator and ground.

Regarding claim 3, Fig. 8 of Partovi H. et al. teaches the dynamic logic RTZ latching mechanism of claim 1, wherein the dynamic evaluator comprises a complex logic circuit (NMOS functions as inverting the input signal and complex compared to a simple inverting logic).

Regarding claim 4, Fig. 8 of Partovi H. et al. teaches the dynamic logic RTZ latching mechanism of claim 1, wherein the delayed inversion logic comprises a series chain of inverters (three inverters connected in series).

Regarding claim 7, Fig. 8 of Partovi H. et al. teaches the dynamic logic RTZ latching mechanism of claim 1, further comprising a footless latching domino circuit having an input coupled to the output node and a registered output node providing a registered output signal (Fig. 8 provides footless full latch comprising two inverters coupled back to back).

Regarding claims 9, Fig. 8 of Partovi H. et al. teaches a dynamic latch circuit, comprising: a dynamic circuit that pre-charges at least one pre-charged node while a clock signal is low (when CLK is low, first PMOS is turned on and precharge the node) and that evaluates a logic function for controlling the state of the at least one pre-charged node when the clock signal goes high (when CLK is high, the precharging is disabled by turning off the first PMOS, and evaluates the input signal D); a delayed inverter receiving the clock signal and providing an inverted delayed clock signal (three

inverters coupled in series provides inverted delayed clock); and a latching circuit (two inverters coupled back to back is a full latch with reset PMOS transistor), coupled to the dynamic circuit and the delayed inverter, that controls the state of an output node based on the state of the at least one pre-charged node during each evaluation period beginning when the clock signal goes high and ending when the inverted delayed clock signal next goes low, and that otherwise asserts the output node to a zero logic state (samples the data on the rising edge of the clock and being reset through PR1 after a predetermined delay period where the output Q is returns to zero when reset by PR1; last paragraph on page 138).

Regarding claim 10, Fig. 8 of Partovi H. et al. teaches the dynamic latch circuit of claim 9, wherein the dynamic circuit comprises: a pull-up device (first PMOS coupled whose gate is coupled to CLK and source coupled to precharge node), coupled to a first pre-charged node, that pre-charges the first pre-charged node while the clock signal is low (when CLK is low, the first PMOS turns on and precharges the source node); a logic circuit (NMOS coupled to D), coupled to the first pre-charged node, that evaluates the logic function (NMOS coupled to D provides inverting logic function); and a pull-down device (NMOS coupled to the output of three inverters coupled in series), coupled to the logic circuit, that enables the logic circuit to evaluate the logic function when the clock signal goes high (when CLK is high, the output of three inverters coupled in series stays high for predetermined delay time set by the three inverters, NMOS is turned on and evaluates; last paragraph on page 138).

Regarding claim 12, Fig. 8 of Partovi H. et al. teaches a dynamic latch circuit of claim 9, wherein the delayed inverter comprises a series chain of inverters (three inverter coupled in series).

Regarding claim 13, Fig. 8 of Partovi H. et al. teaches a dynamic latch circuit of claim 9, further comprising a footless latching domino circuit coupled to the output node that provides a corresponding registered output (Fig. 8 provides footless full latch comprising two inverters coupled back to back).

Regarding claims 18, Fig. 8 of Partovi H. et al. teaches a dynamic logic RTZ latching method, comprising: pre-setting a first node while a clock signal is in a first logic state (when CLK is low, the first PMOS turns on and precharges the source node to logic high); dynamically evaluating a logic function to control the logic state of the first node when the clock signal transitions to a second logic state (when CLK is high, the precharging is disabled by turning off the first PMOS, and evaluates the input signal D); delaying and inverting the clock signal and providing a delayed inverted clock signal (three inverters coupled in series provides inverted delayed clock); latching a logic state of an output node based on the logic state of the first node determined during an evaluation period beginning when the clock signal transitions to the second logic state and ending with the next corresponding transition of the delayed inverted clock signal;

and returning the logic state of the output node to a low logic state between evaluation periods (samples the data on the rising edge of the clock and being reset through PR1 after a predetermined delay period where the output Q is returns to zero when reset by PR1; last paragraph on page 138).

Regarding claims 19, Fig. 8 of Partovi H. et al. teaches the method of claim 18, wherein the pre-setting a first node comprises pre-charging the first node to a high logic state (when CLK is low, the first PMOS turns on and precharges the source node to logic high).

Regarding claim 20, Fig. 8 of Partovi H et al. teaches the method of claim 18, further comprising adding a latching domino circuit to the output node to provide a registered output signal (Fig. 8 provides footless full latch comprising two inverters coupled back to back).

Allowable Subject Matter

Claims 5-6, 8, 11, 14-17, and 21-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Partovi H et al. teaches a single-ended dynamic hybrid latch-flipflop, one of ordinary skill in the art would not have been motivated to modify the teaching of

Partovi H et al. to further includes, among other things, the specific of an N-channel pass device having a gate receiving the evaluation complete signal and a drain and source coupled between the pre-charged node and a pull-up control node (claim 5), a third N-channel device having a gate coupled to the control node and a drain and source coupled between the intermediate node and ground (claim 8), a pass device that couples a second node to the at least one pre-charged node when the inverted delayed clock signal is high (claim 11), the latching circuit comprising a plurality of latching circuits, each coupled to a corresponding one of the plurality of dynamic circuits, each receiving a corresponding one of the plurality of input signals, and each having an output that is wire-ORed coupled to the output node (claim 14), and passing a logic state of the first node to a pull-up control node while the delayed inverted clock signal is in a high logic state (claim 21).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chen et al. (US PAT No. 6,181,180) discloses a low power high performance flip-flop.

Mikan, Jr. et al. (US PAT No. 6,111,444) discloses an edge triggered latch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on Monday-Friday 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819